[Claim 1]   1. A method of forming a split programming virtual ground (SPVG) SONOS memory, comprising:

providing a substrate having at least a first conductive type well positioned in the substrate, and a plurality of select gate structures arranged in parallel and positioned on the first conductive type well;
forming a plurality of sacrificial spacers alongside each select gate structure;
performing an implantation process by utilizing the select gate structures and the sacrificial spacers as a mask to form a second conductive type doped region in the first conductive type well between two adjacent select gate structures;
removing the sacrificial spacers;
forming a composite dielectric layer covering the select gate structures; and
forming a plurality of word lines perpendicular to the select gate structures on the composite dielectric layer.

[Claim 2]   2. The method of claim 1, wherein each select gate structure from bottom to top comprises a gate insulating layer, a polysilicon layer, and a cap layer.

[Claim 3]   3. The method of claim 1, wherein the second conductive type doped regions serve as buried bit lines.

[Claim 4]   4. The method of claim 1, wherein the composite dielectric layer is an ONO tri-layer dielectric.

[Claim 5]   5. The method of claim 1, wherein the first conductive type well is a P well.

[Claim 6]   6. The method of claim 5, wherein each second conductive type doped region is an N doped region.

[Claim 7]   7. A method of forming a dual-bit storage nonvolatile memory, comprising:

providing a plurality of select gate structures arranged in parallel on the substrate;
forming a sacrificial spacer alongside each select gate structure;
performing an implantation process by utilizing the select gate structures and the sacrificial spacers as a mask to form a doped region in the substrate between any two adjacent select gate structures;
removing the sacrificial spacers;
forming a composite dielectric layer covering the select gate structures; and
forming a plurality of word lines perpendicular to the select gate structures on the composite dielectric layer.

[Claim 8]   8. The method of claim 7, wherein each select gate structure from bottom to top comprises a gate insulating layer and a conductive layer.

[Claim 9]   9. The method of claim 8, wherein the conductive layer is a polysilicon layer, and the nonvolatile memory is a split programming virtual ground (SPVC) SONOS memory.

[Claim 10] 10.   The method of claim 8, wherein the conductive layer is a metal layer, and the nonvolatile memory is a split programming virtual ground (SPVC) MONOS memory.

[Claim 11] 11.   The method of claim 7, wherein each select gate structure further comprises a cap layer positioned on the conductive layer.

[Claim 12]   12.   The method of claim 7, wherein the substrate further comprises a linear oxide layer positioned on the substrate and covering each select gate structure.

[Claim 13]   13.   The method of claim 7, wherein the doped regions serve as buried bit lines.

[Claim 14]   14.   The method of claim 7, wherein the composite dielectric layer is an ONO tri-layer dielectric.

[Claim 15]   15.   The method of claim 7, wherein the substrate further comprises at least a well, and the select gate structures are positioned on the well.

[Claim 16]   16.   The method of claim 15, wherein the well is a P well, and each doped region is an N doped region.